FIG. 1

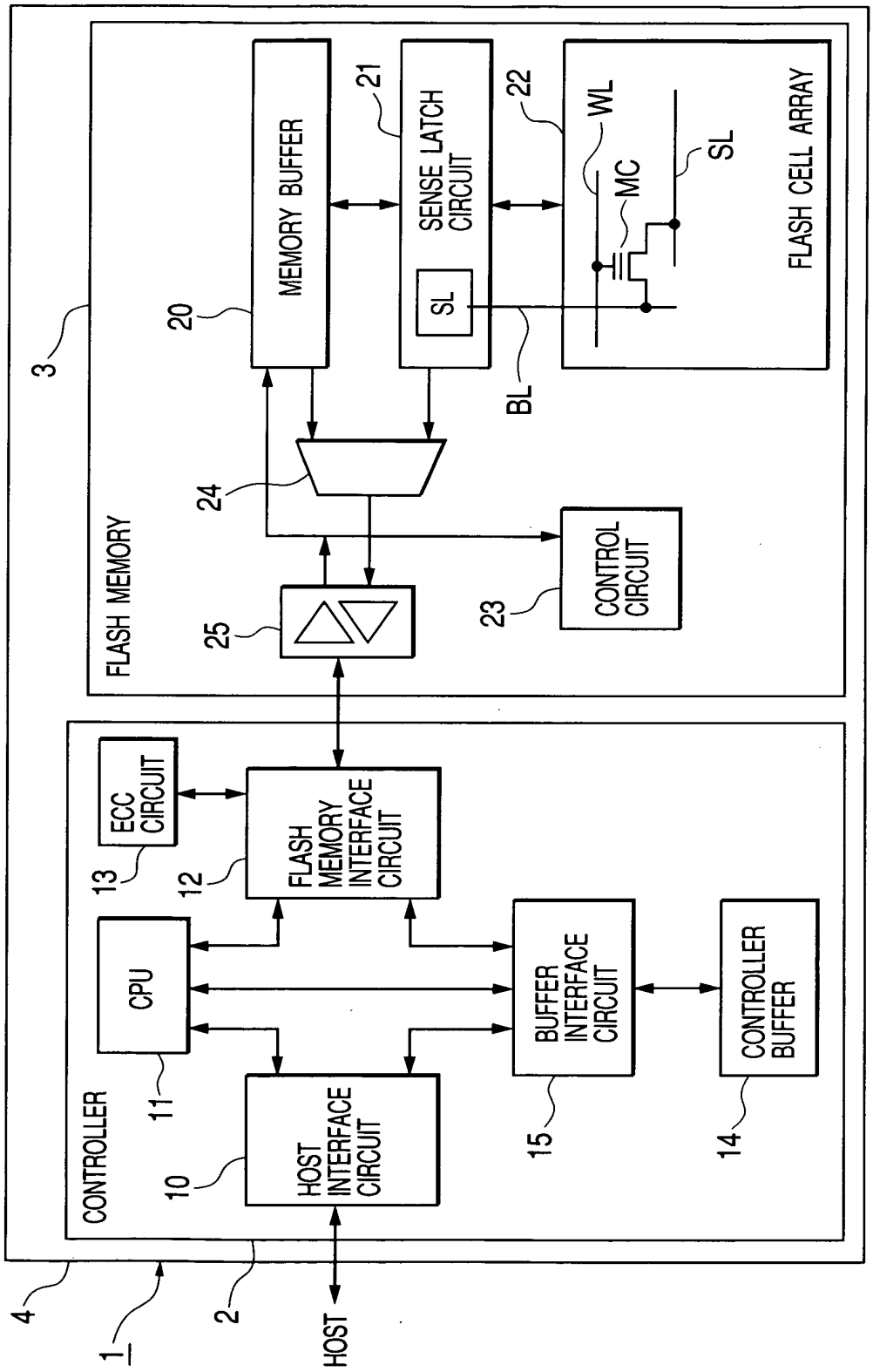

HOST
1
2
4
CONTROLLER
HOST INTERFACE CIRCUIT
10
CPU
11
ECC CIRCUIT
13
FLASH MEMORY INTERFACE CIRCUIT
12
BUFFER INTERFACE CIRCUIT
15
CONTROLLER BUFFER
14
3
FLASH MEMORY
MEMORY BUFFER
20
SENSE LATCH CIRCUIT
21
SL
BL
FLASH CELL ARRAY
22
WL
MC
SL
24
25
CONTROL CIRCUIT
23

FIG. 2

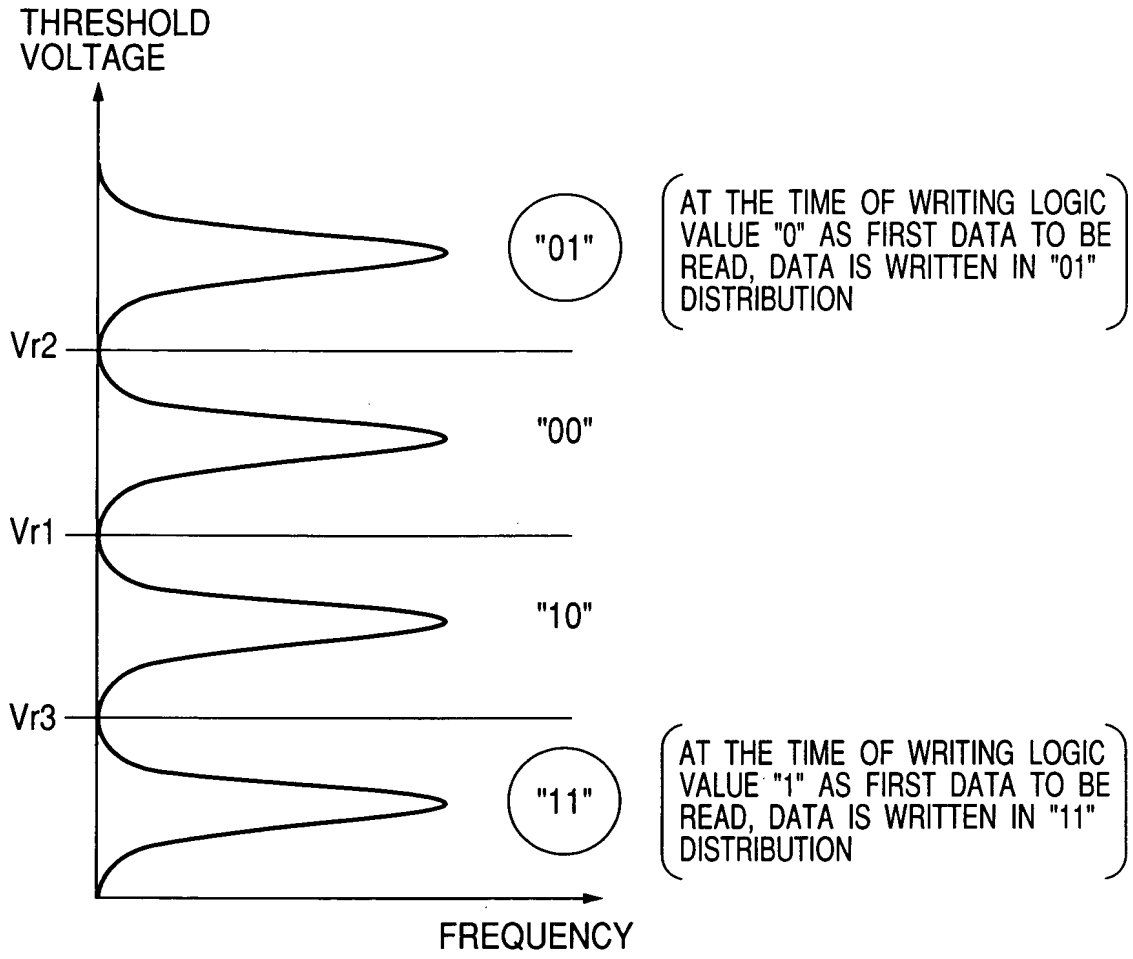

THRESHOLD VOLTAGE
"01"
AT THE TIME OF WRITING LOGIC VALUE "0" AS FIRST DATA TO BE READ, DATA IS WRITTEN IN "01" DISTRIBUTION
Vr2
"00"
Vr1
"10"
Vr3
"11"
AT THE TIME OF WRITING LOGIC VALUE "1" AS FIRST DATA TO BE READ, DATA IS WRITTEN IN "11" DISTRIBUTION
FREQUENCY

FIG. 3

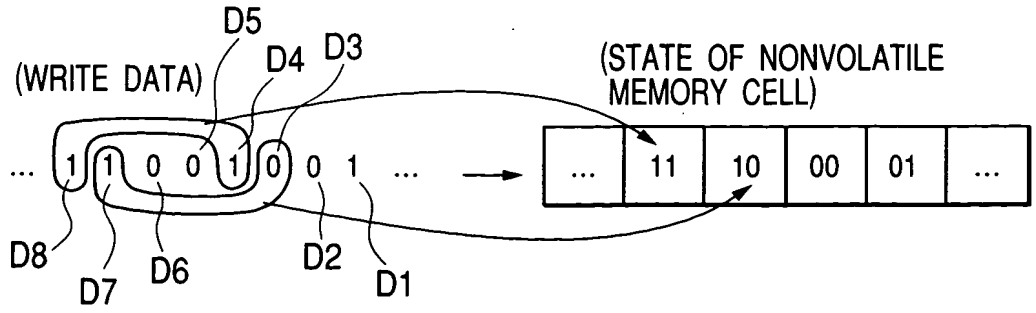

D5
D4
D3
(WRITE DATA)
(STATE OF NONVOLATILE MEMORY CELL)
... 1 1 0 0 1 0 0 1 ...
... 11 10 00 01 ...
D8
D7
D6
D2
D1

FIG. 4

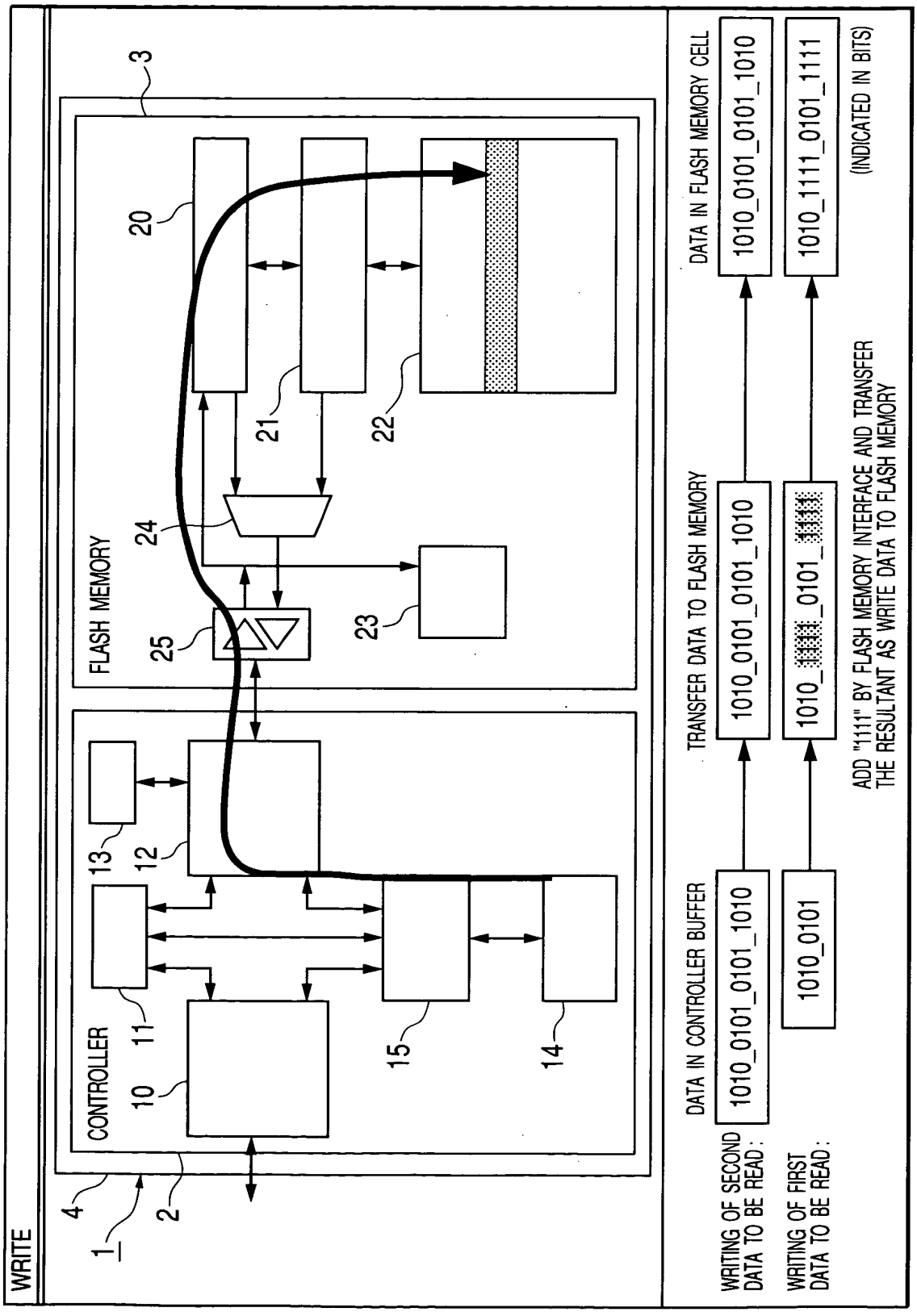

WRITE
1
2
4
CONTROLLER
10
11
12
13
14
15
FLASH MEMORY
3
20
21
22
23
24
25
DATA IN CONTROLLER BUFFER
TRANSFER DATA TO FLASH MEMORY
DATA IN FLASH MEMORY CELL
WRITING OF SECOND DATA TO BE READ:
1010_0101_0101_1010
1010_0101_0101_1010
1010_0101_0101_1010
WRITING OF FIRST DATA TO BE READ:
1010_0101
1010_1111_0101_1111
(INDICATED IN BITS)
ADD "1111" BY FLASH MEMORY INTERFACE AND TRANSFER THE RESULTANT AS WRITE DATA TO FLASH MEMORY

FIG. 5

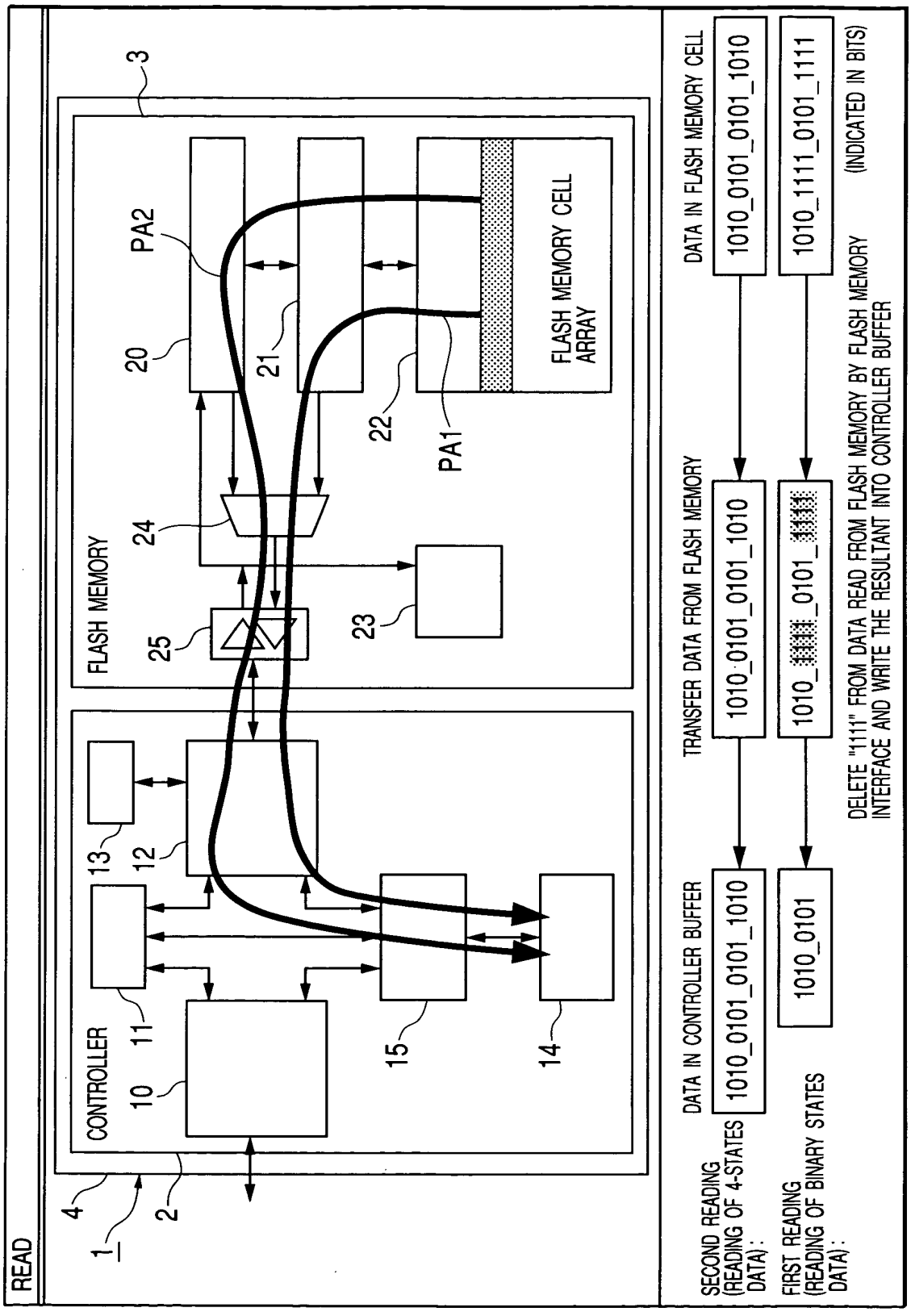

READ
1
2
4
CONTROLLER
10
11
12
13
14
15
FLASH MEMORY
3
PA2
20
21
22
PA1
FLASH MEMORY CELL ARRAY
23
24
25
DATA IN CONTROLLER BUFFER
SECOND READING (READING OF 4-STATES DATA):
1010_0101_0101_1010
FIRST READING (READING OF BINARY STATES DATA):
1010_0101
TRANSFER DATA FROM FLASH MEMORY
DATA IN FLASH MEMORY CELL
1010_0101_0101_1010
1010_1111_0101_1111
DELETE "111" FROM DATA READ FROM FLASH MEMORY BY FLASH MEMORY INTERFACE AND WRITE THE RESULTANT INTO CONTROLLER BUFFER
(INDICATED IN BITS)

FIG. 6

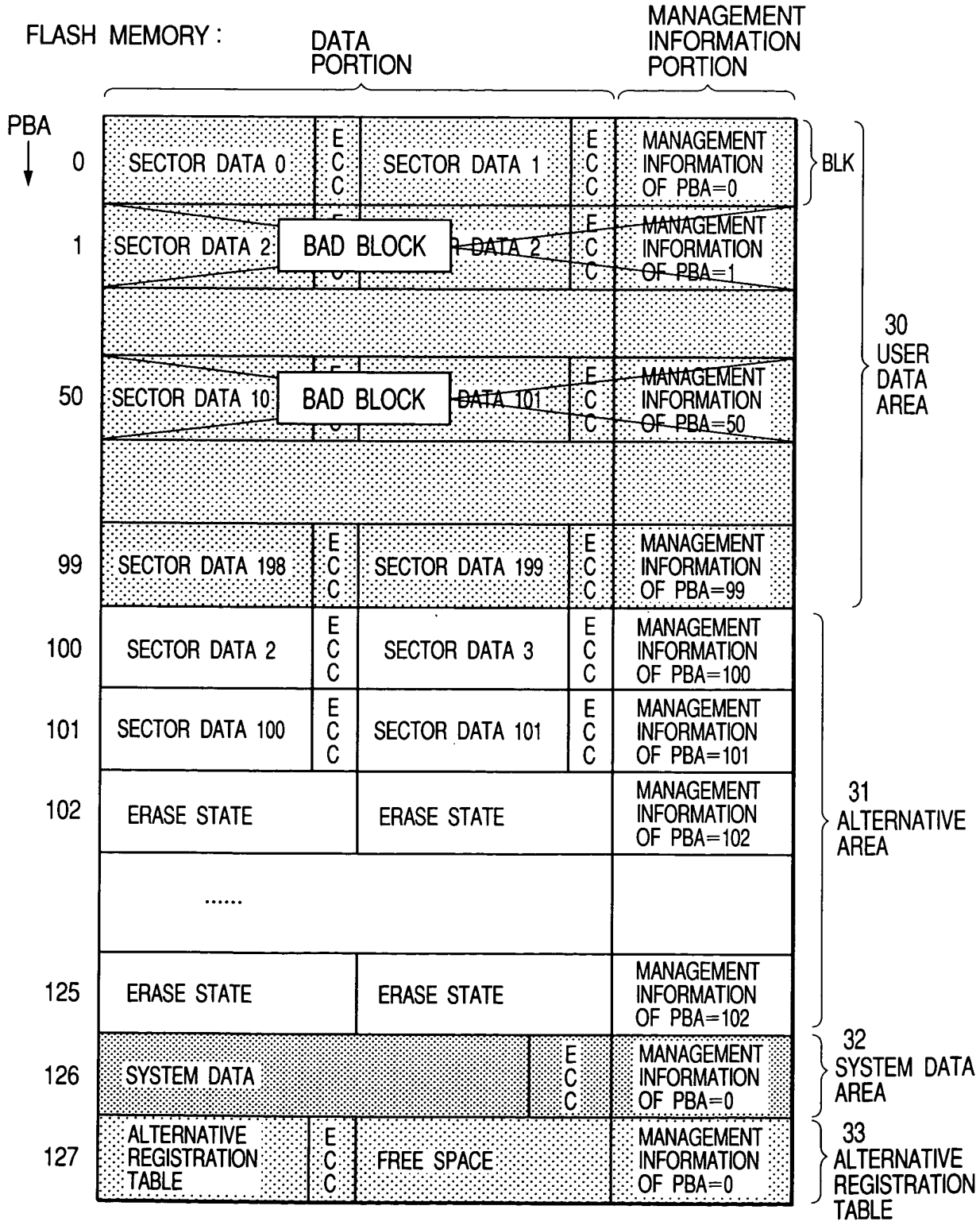

FLASH MEMORY :
DATA PORTION
MANAGEMENT INFORMATION PORTION
PBA
0
SECTOR DATA 0
ECC
SECTOR DATA 1
ECC
MANAGEMENT INFORMATION OF PBA=0
BLK
1
SECTOR DATA 2
BAD BLOCK
DATA 2
ECC
MANAGEMENT INFORMATION OF PBA=1
50
SECTOR DATA 10
BAD BLOCK
DATA 101
ECC
MANAGEMENT INFORMATION OF PBA=50
30 USER DATA AREA
99
SECTOR DATA 198
ECC
SECTOR DATA 199
ECC
MANAGEMENT INFORMATION OF PBA=99
100
SECTOR DATA 2
ECC
SECTOR DATA 3
ECC
MANAGEMENT INFORMATION OF PBA=100
101
SECTOR DATA 100
ECC
SECTOR DATA 101
ECC
MANAGEMENT INFORMATION OF PBA=101
102
ERASE STATE
ERASE STATE
MANAGEMENT INFORMATION OF PBA=102
.....
125
ERASE STATE
ERASE STATE
MANAGEMENT INFORMATION OF PBA=102
31 ALTERNATIVE AREA
126
SYSTEM DATA
ECC
MANAGEMENT INFORMATION OF PBA=0
32 SYSTEM DATA AREA
127
ALTERNATIVE REGISTRATION TABLE
ECC
FREE SPACE
MANAGEMENT INFORMATION OF PBA=0
33 ALTERNATIVE REGISTRATION TABLE

FIG. 7

ALTERNATIVE REGISTRATIION TABLE :

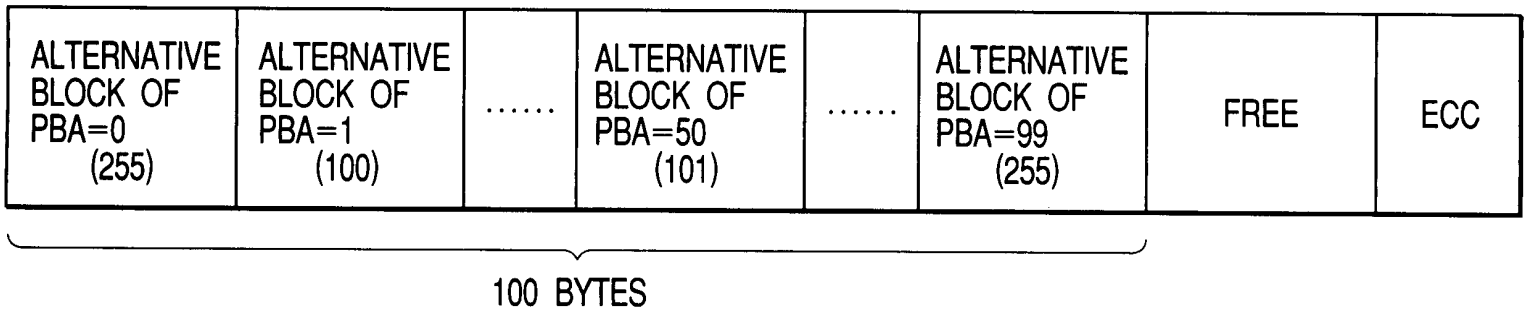


FIG. 8

MANAGEMENT INFORMATION :

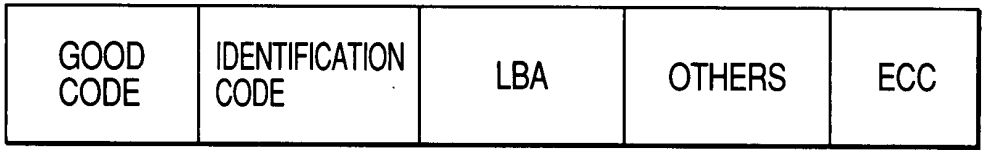


FIG. 9

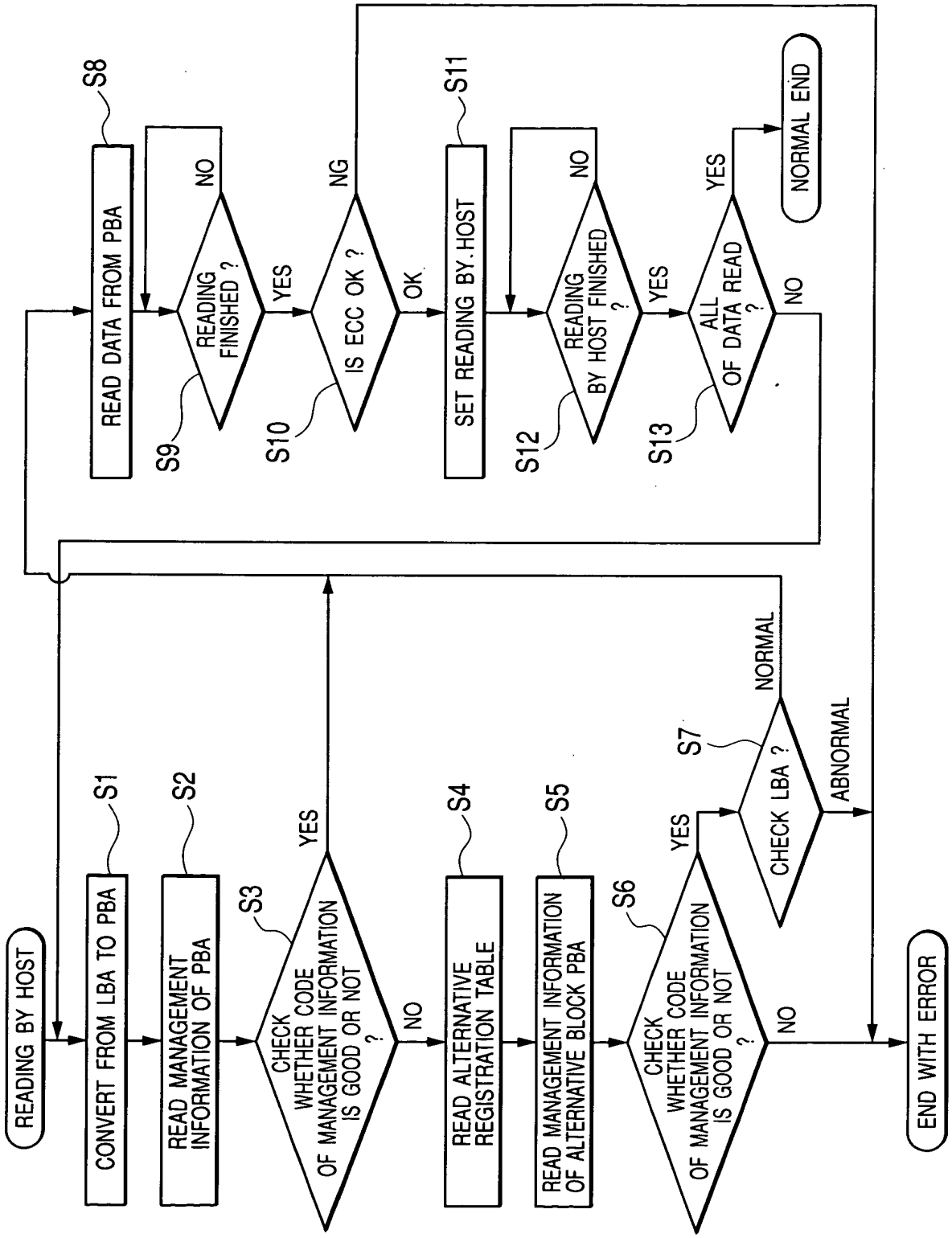

READING BY HOST
S1
CONVERT FROM LBA TO PBA
S2
READ MANAGEMENT INFORMATION OF PBA
S3
CHECK WHETHER CODE OF MANAGEMENT INFORMATION IS GOOD OR NOT ?
YES
NO
S4
READ ALTERNATIVE REGISTRATION TABLE
S5
READ MANAGEMENT INFORMATION OF ALTERNATIVE BLOCK PBA
S6
CHECK WHETHER CODE OF MANAGEMENT INFORMATION IS GOOD OR NOT ?
YES
NO
S7
CHECK LBA ?
NORMAL
ABNORMAL
END WITH ERROR
S8
READ DATA FROM PBA
S9
READING FINISHED ?
NO
YES
S10
IS ECC OK ?
NG
OK
S11
SET READING BY. HOST
S12
READING BY HOST FINISHED ?
NO
YES
S13
ALL OF DATA READ ?
YES
NO
NORMAL END

FIG. 10

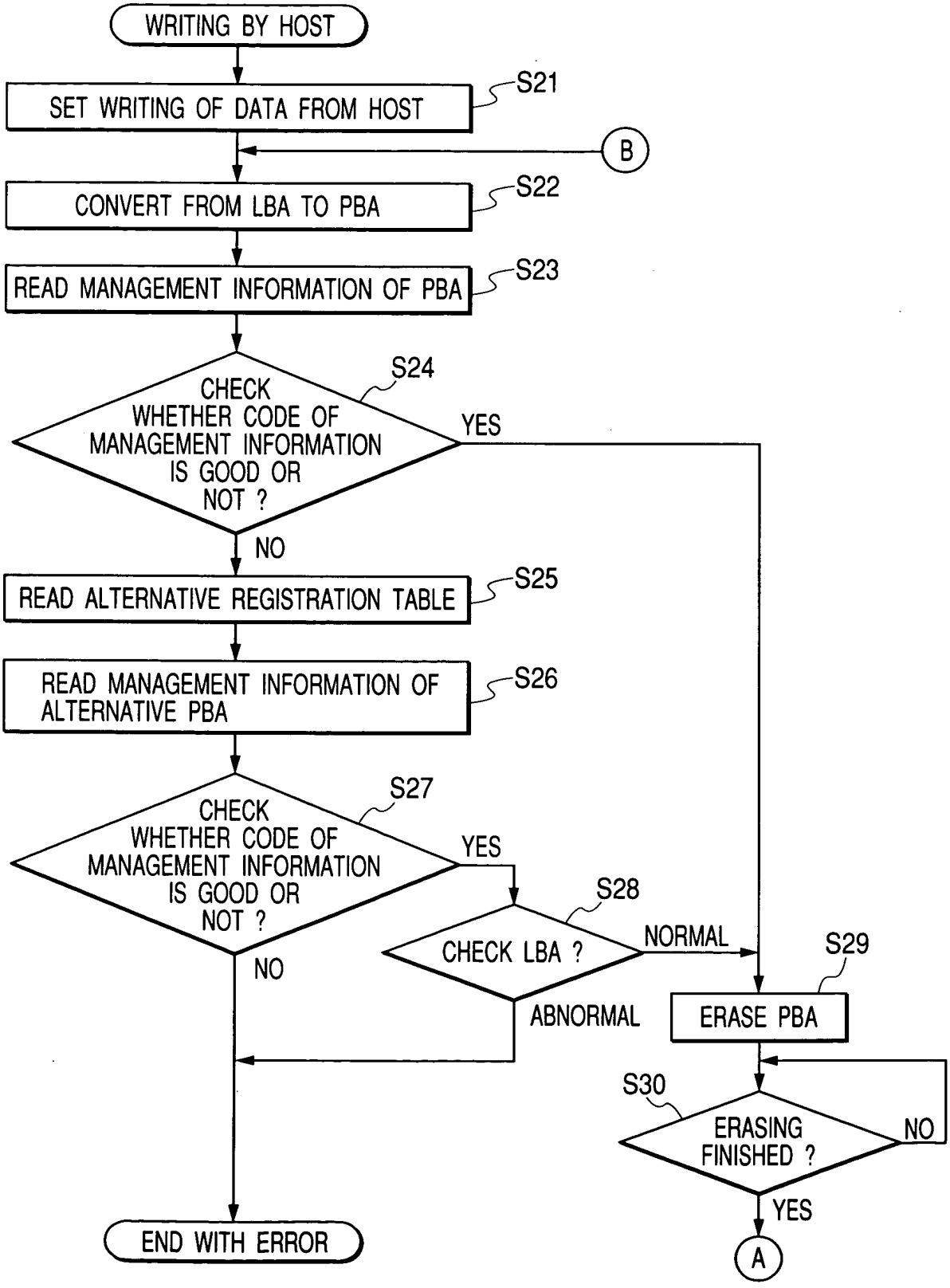

WRITING BY HOST
SET WRITING OF DATA FROM HOST
S21
B
CONVERT FROM LBA TO PBA
S22
READ MANAGEMENT INFORMATION OF PBA
S23
CHECK WHETHER CODE OF MANAGEMENT INFORMATION IS GOOD OR NOT ?
S24
YES
NO
READ ALTERNATIVE REGISTRATION TABLE
S25
READ MANAGEMENT INFORMATION OF ALTERNATIVE PBA
S26
CHECK WHETHER CODE OF MANAGEMENT INFORMATION IS GOOD OR NOT ?
S27
YES
NO
CHECK LBA ?
S28
NORMAL
ABNORMAL
S29
ERASE PBA
S30
ERASING FINISHED ?
NO
YES
A
END WITH ERROR

FIG. 11

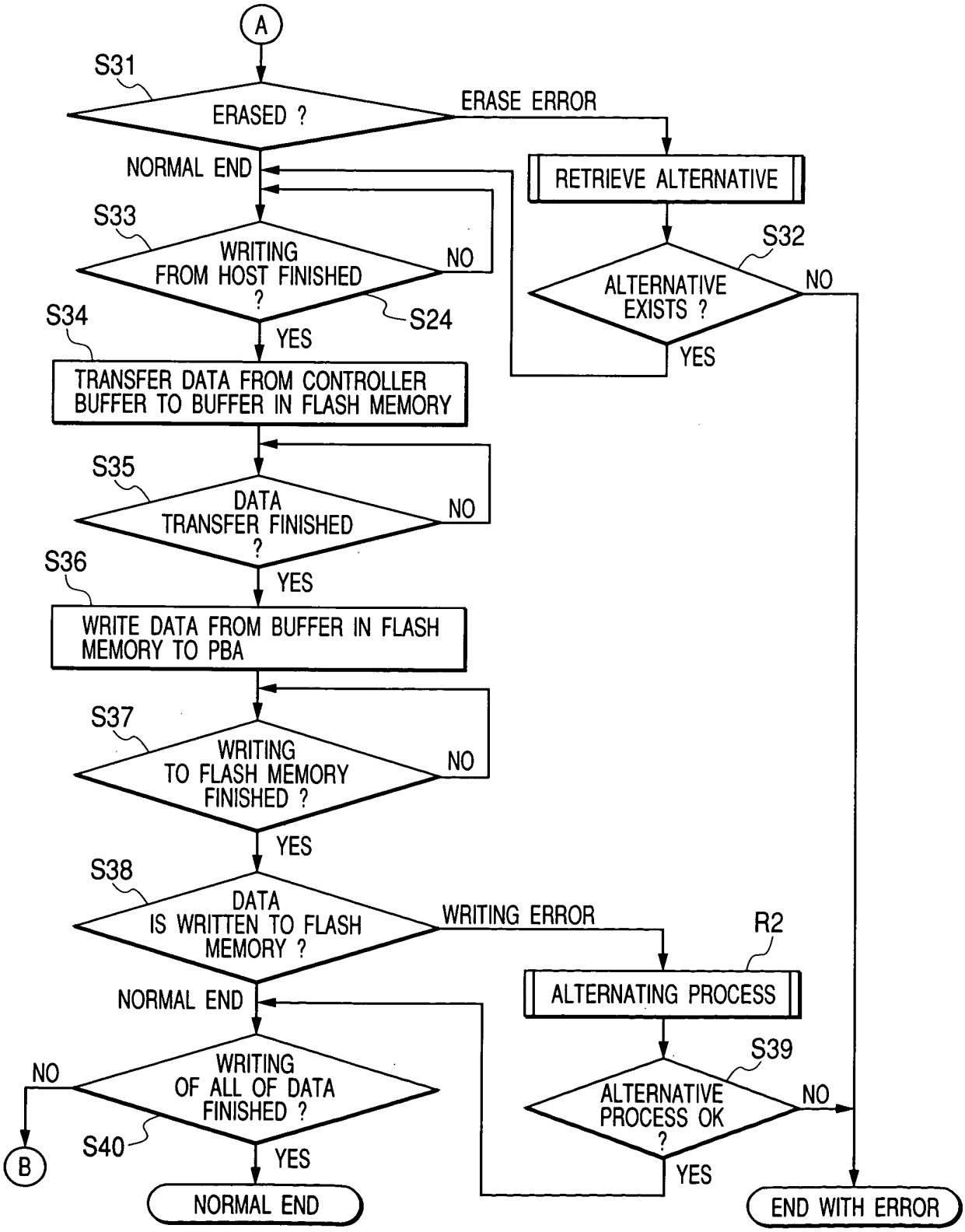

A
S31
ERASED ?
ERASE ERROR
NORMAL END
RETRIEVE ALTERNATIVE
S33
WRITING FROM HOST FINISHED ?
NO
S24
S32
ALTERNATIVE EXISTS ?
NO
YES
S34
YES
TRANSFER DATA FROM CONTROLLER BUFFER TO BUFFER IN FLASH MEMORY
S35
DATA TRANSFER FINISHED ?
NO
S36
YES
WRITE DATA FROM BUFFER IN FLASH MEMORY TO PBA
S37
WRITING TO FLASH MEMORY FINISHED ?
NO
YES
S38
DATA IS WRITTEN TO FLASH MEMORY ?
WRITING ERROR
R2
ALTERNATING PROCESS
NORMAL END
S39
ALTERNATIVE PROCESS OK ?
NO
YES
NO
WRITING OF ALL OF DATA FINISHED ?
S40
YES
B
NORMAL END
END WITH ERROR

FIG. 12

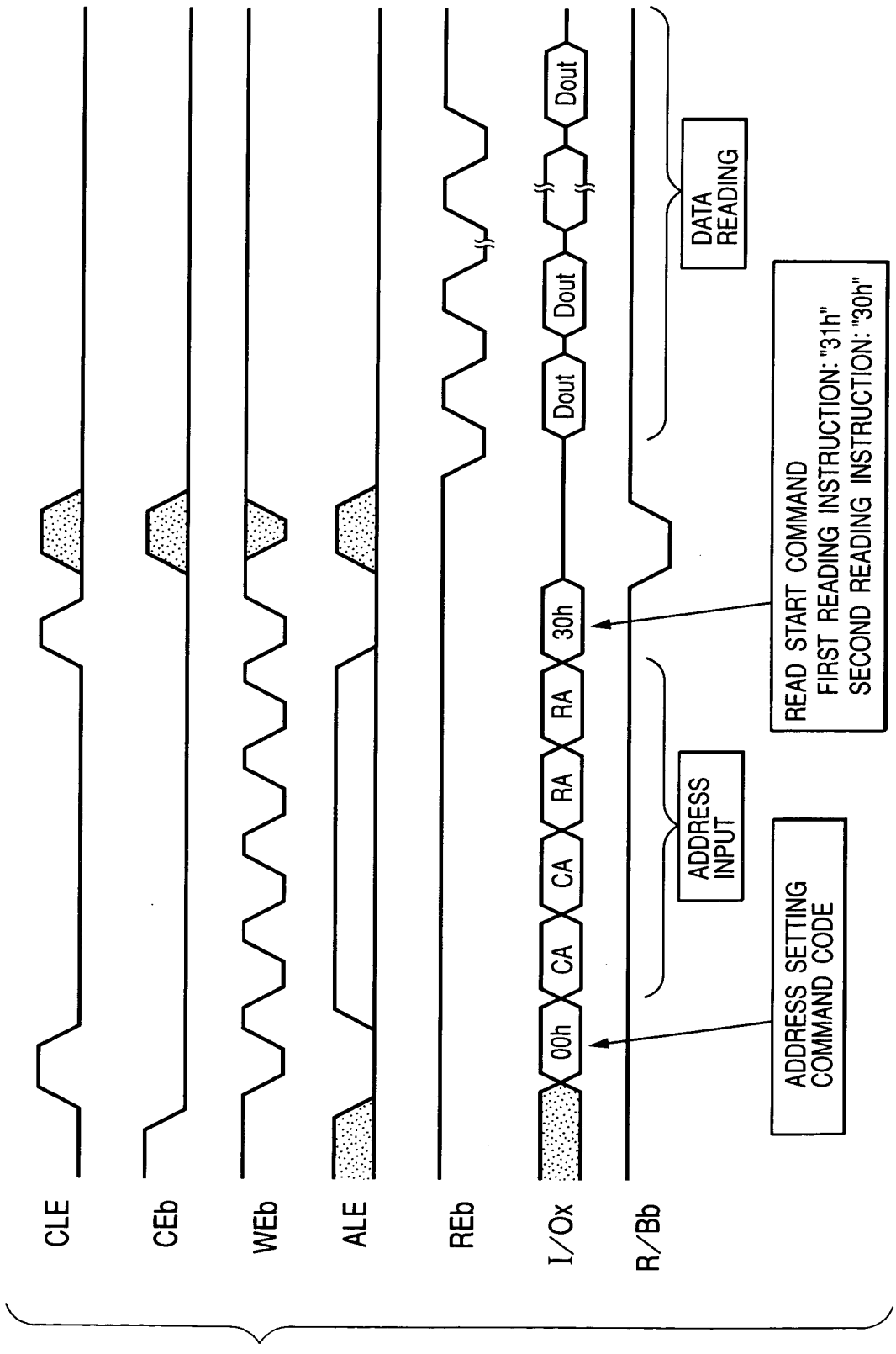

CLE
CEb
WEb
ALE
REb
I/Ox
R/Bb
00h
CA
CA
RA
RA
30h
Dout
Dout
Dout
Dout
ADDRESS SETTING COMMAND CODE
ADDRESS INPUT
READ START COMMAND
FIRST READING INSTRUCTION: "31h"
SECOND READING INSTRUCTION: "30h"
DATA READING

FIG. 13

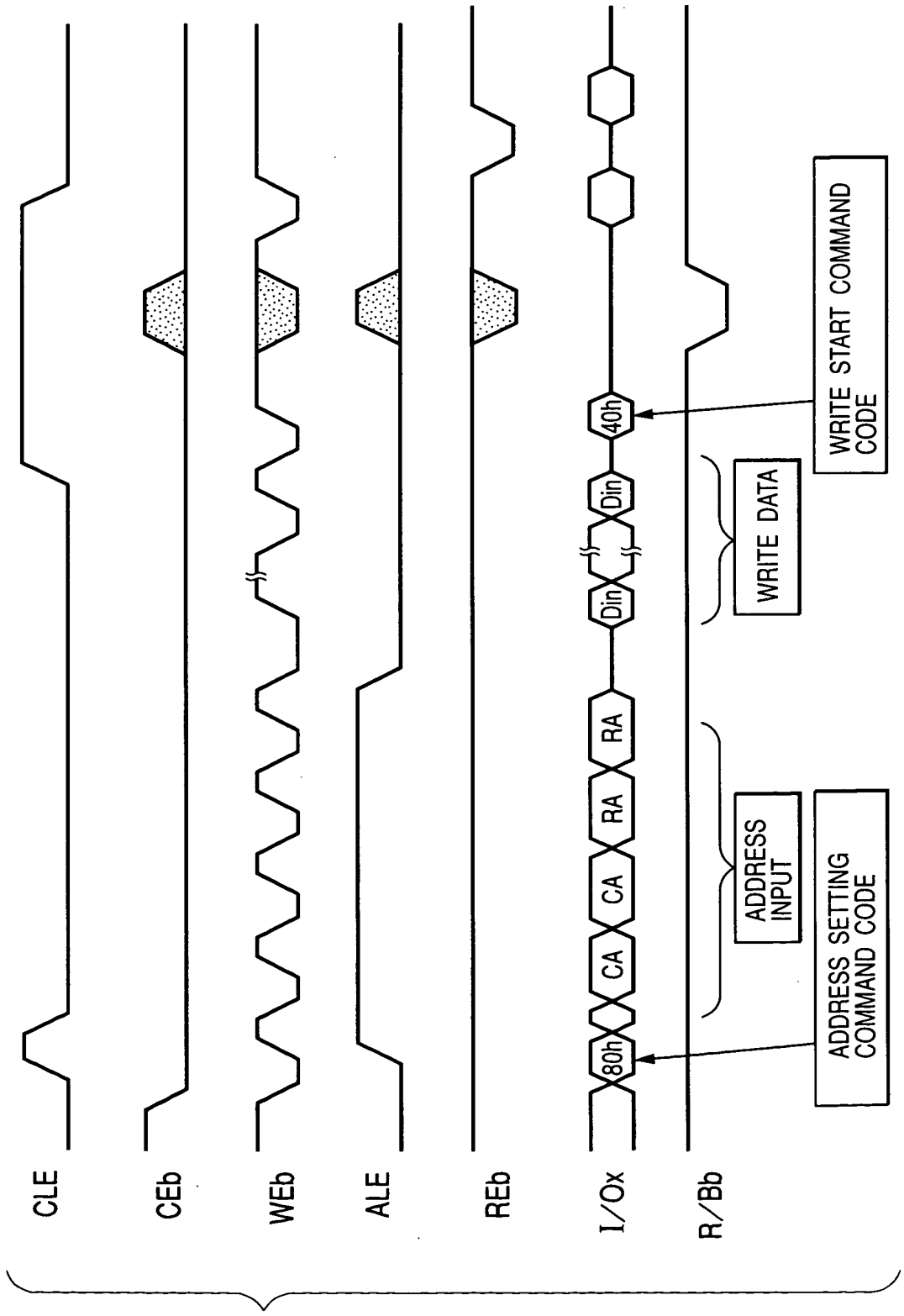

CLE
CEb
WEb
ALE
REb
I/Ox
R/Bb
80h
CA
CA
RA
RA
Din
Din
40h
ADDRESS SETTING COMMAND CODE
ADDRESS INPUT
WRITE DATA
WRITE START COMMAND CODE

FIG. 14

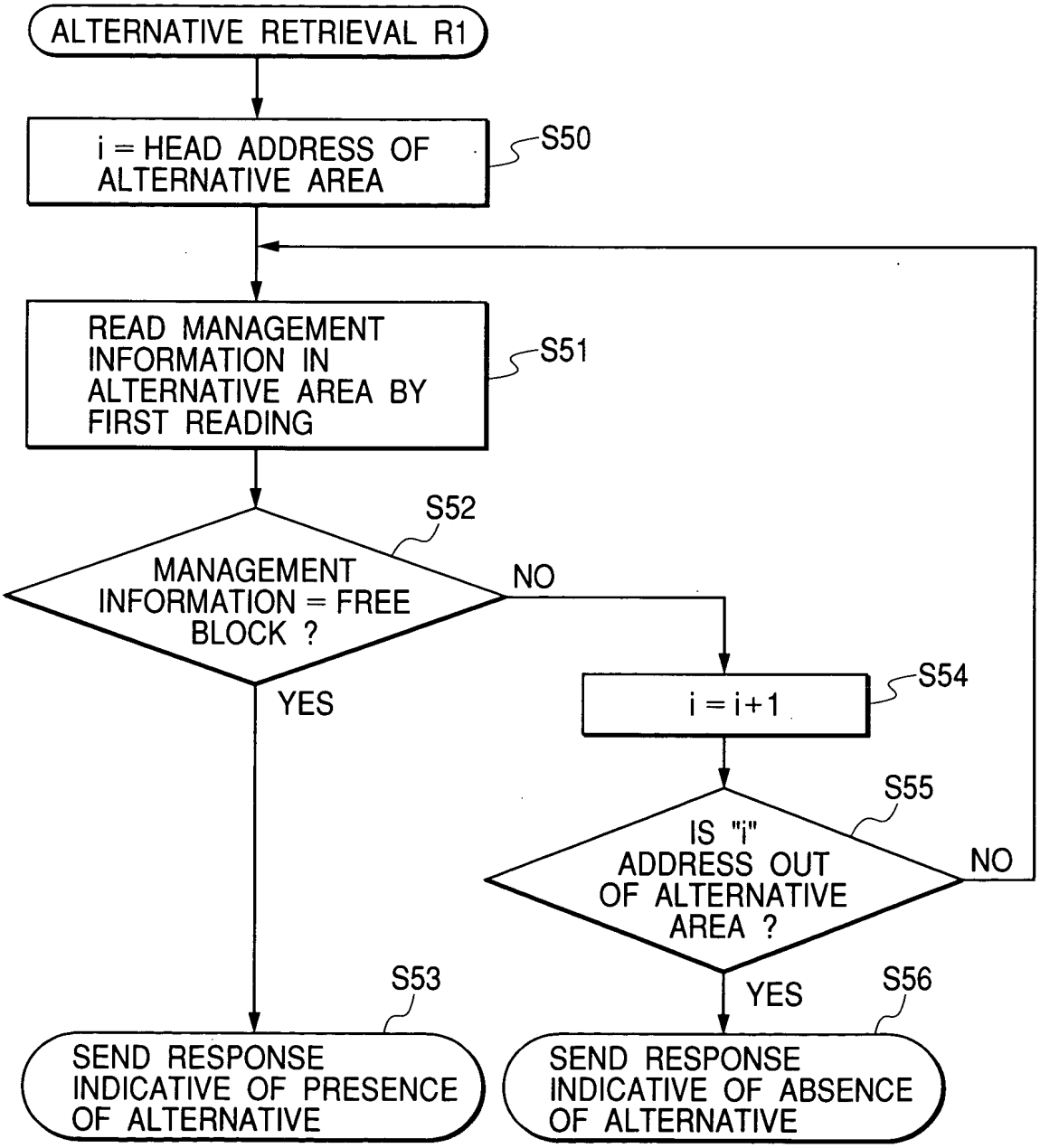

ALTERNATIVE RETRIEVAL R1
i = HEAD ADDRESS OF ALTERNATIVE AREA
S50
READ MANAGEMENT INFORMATION IN ALTERNATIVE AREA BY FIRST READING
S51
S52
MANAGEMENT INFORMATION = FREE BLOCK ?
NO
YES
i = i+1
S54
S55
IS "i" ADDRESS OUT OF ALTERNATIVE AREA ?
NO
YES
S53
S56
SEND RESPONSE INDICATIVE OF PRESENCE OF ALTERNATIVE
SEND RESPONSE INDICATIVE OF ABSENCE OF ALTERNATIVE

FIG. 15

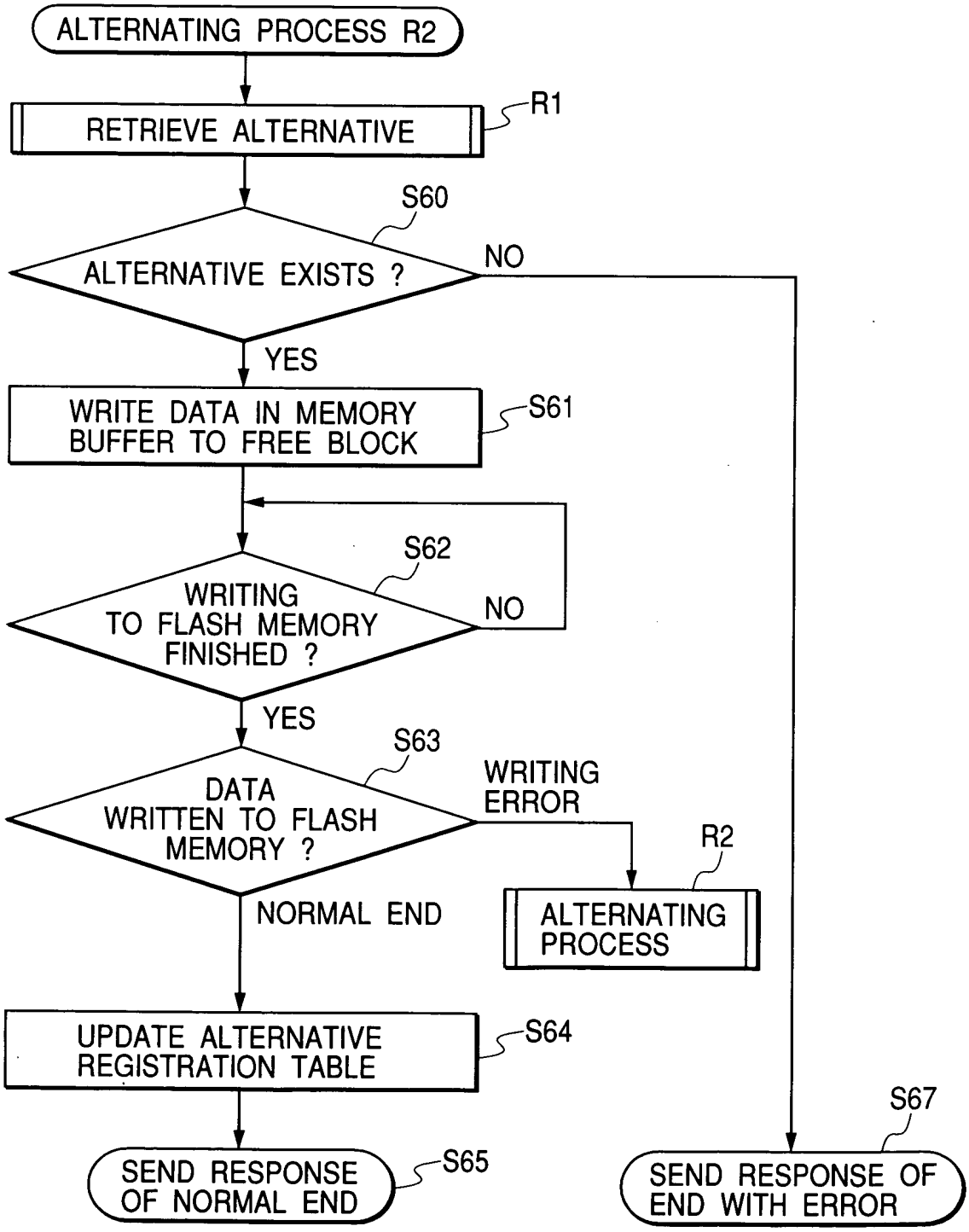
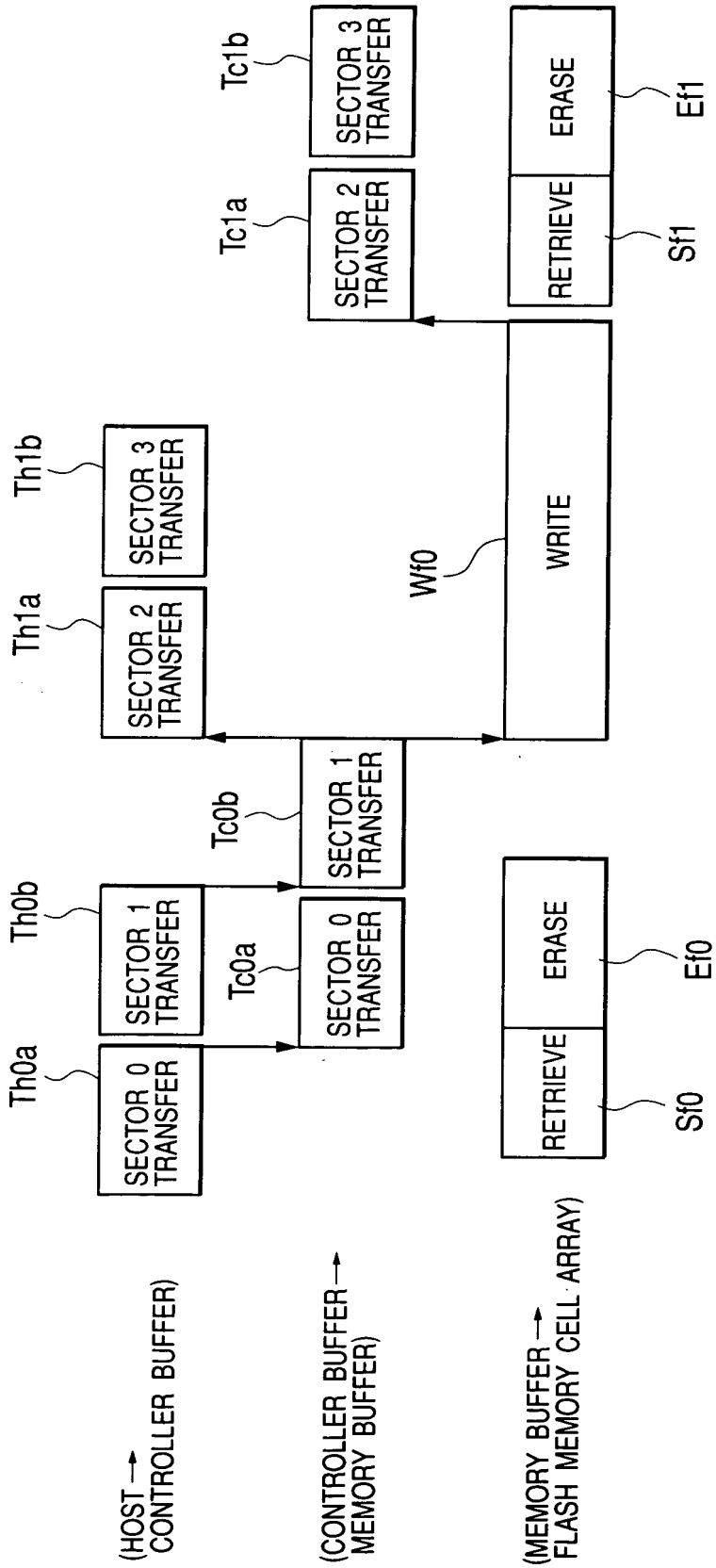

ALTERNATING PROCESS R2
RETRIEVE ALTERNATIVE
R1
S60
ALTERNATIVE EXISTS ?
NO
YES
WRITE DATA IN MEMORY BUFFER TO FREE BLOCK
S61
S62
WRITING TO FLASH MEMORY FINISHED ?
NO
YES
S63
DATA WRITTEN TO FLASH MEMORY ?
WRITING ERROR
R2
ALTERNATING PROCESS
NORMAL END
UPDATE ALTERNATIVE REGISTRATION TABLE
S64
SEND RESPONSE OF NORMAL END
S65
S67
SEND RESPONSE OF END WITH ERROR

FIG. 16


(HOST → CONTROLLER BUFFER)
(CONTROLLER BUFFER → MEMORY BUFFER)
(MEMORY BUFFER → FLASH MEMORY CELL ARRAY)
Th0a
SECTOR 0 TRANSFER
Th0b
SECTOR 1 TRANSFER
Th1a
SECTOR 2 TRANSFER
Th1b
SECTOR 3 TRANSFER
Tc0a
SECTOR 0 TRANSFER
Tc0b
SECTOR 1 TRANSFER
Tc1a
SECTOR 2 TRANSFER
Tc1b
SECTOR 3 TRANSFER
Wf0
WRITE
Sf0
RETRIEVE
Ef0
ERASE
Sf1
RETRIEVE
Ef1
ERASE